

Verification CoStart: Low Power

Accelerate low power verification with Synopsys tool and methodology experts

Overview

Adoption of low power design techniques is growing rapidly to enable ASICs and SoCs to support the advanced power management required across today's electronic products, from mobile devices to servers and networking. Advanced low power techniques such as Power Gating, Retention, Low-VDD Standby, and Dynamic Voltage Scaling (DVS) employ voltage control to enable fine-grained power management. Designs are partitioned into power domains that can be separately controlled by one or more of these low power design techniques. Increasingly stringent power requirements have necessitated the use of multiple supply voltages. Low power designs typically operate in different modes, with each mode corresponding to one or more power states. Comprehensive verification of low power designs requires verification not just in all the power states, but also of the specified transitions and transition sequencing between power states as the design moves from one operating mode to another. A single bug in any of these incredibly complex scenarios may cause functional failures in silicon.

To meet these needs, customers are adding low power enabled simulation as well as static checking to their verification flows. While many customers are now very well versed with these techniques, many are just ramping-up, which is impacting project schedules and potentially leaving bugs undetected.

About Verification CoStart for Low Power

Verification CoStart enables customers to accelerate adoption of new technologies and increases productivity in their verification environments.

Verification CoStart for Low Power is a 10-day service where Synopsys engages with the customer's Low Power team to accelerate their knowledge of low power design techniques leveraging Synopsys VC LP and VCS NLP. Synopsys consultants will assist the customer in setting up their low power static checking flow and simulation environment. Synopsys consultants will bring up a couple of blocks with the customer's engineers to ensure that the customer can leverage the tools in a production setting. To complete the services engagement, Synopsys will provide hands-on training for up to five customer engineers on how-to run the tool, as well as debugging and interpreting the results.



Verification CoStart Low Power Services

As part of the engagement, Synopsys experts will work closely with customer's engineers to enable the following:

- Introduction to UPF
- Writing UPF
- Review existing LP Verification methodology and suggest improvements
- Static checking at RTL with VC LP
- Static checking on Netlist/PG with VC LP
- Writing custom checks, debug using Tcl with VC LP
- Running Hierarchical Signoff Abstraction Model (SAM) flow with VC LP
- Using machine learning-based root cause analysis (RCA) feature with VC LP
- Power aware simulations using VCS NLP
- Writing power aware testbench using VCS NLP
- Debugging low power issues with Verdi
- Running power aware gate level simulations
- Writing advanced low power assertions using VCS NLP
- Achieving low power coverage using VCS NLP

Assumptions and Dependencies

- Customer's engineers will be available for consultation with Synopsys consultants.
- Synopsys engineers will have access to customer's design environment either directly or through a customer's engineer.
- Customer has identified the engineers who will go through the hands-on training program.

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000